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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/615,794	07/13/2000	Dong-Gyu Kim	06192.0141.NPUS00	5256

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EXAMINER	
RUDE, TIMOTHY L	
ART UNIT	**PAPER NUMBER**
2883	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/615,794	KIM, DONG-GYU	
	Examiner	Art Unit	
	Timothy L. Rude	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-51* is/are pending in the application.

4a) Of the above claim(s) *5-7,16-18 and 25-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9,11-13,15 and 20-24* is/are rejected.

7)☐ Claim(s) *8,14 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 27 October 2004 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 9, 11-13, 15, and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukada et al (Tsukada) USPAT 4,955,697 in view of Shimada et al (Shimada) USPAT 5,877,830.

As to claims 1-3, Tsukada discloses in Figure 10 his fourth embodiment (col. 8, lines 38-62) a liquid crystal display, comprising:

a first insulating substrate;

a plurality of gate lines, 3, formed at the first substrate to transmit scanning signals;

a plurality data lines, 1, crossing over the gate lines to transmit picture signals;

a plurality of pixels defined by the gate lines and data lines, the gate lines dividing the pixel electrode into rows and the data lines dividing the pixel electrodes into columns;

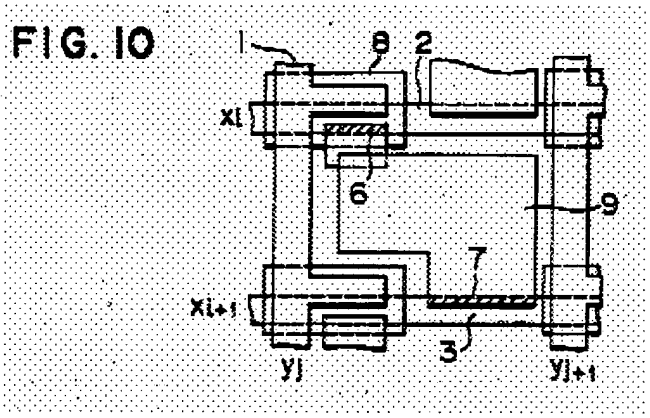
pixel electrodes corresponding to one of the plurality of pixels;

a second insulating substrate facing the first substrate;

a liquid crystal layer injected into the gap between said first insulating substrate and said second insulating substrate; and

a storage capacitor, 7, formed between said pixel electrode and the previous gate line (col. 6, lines 40-48).

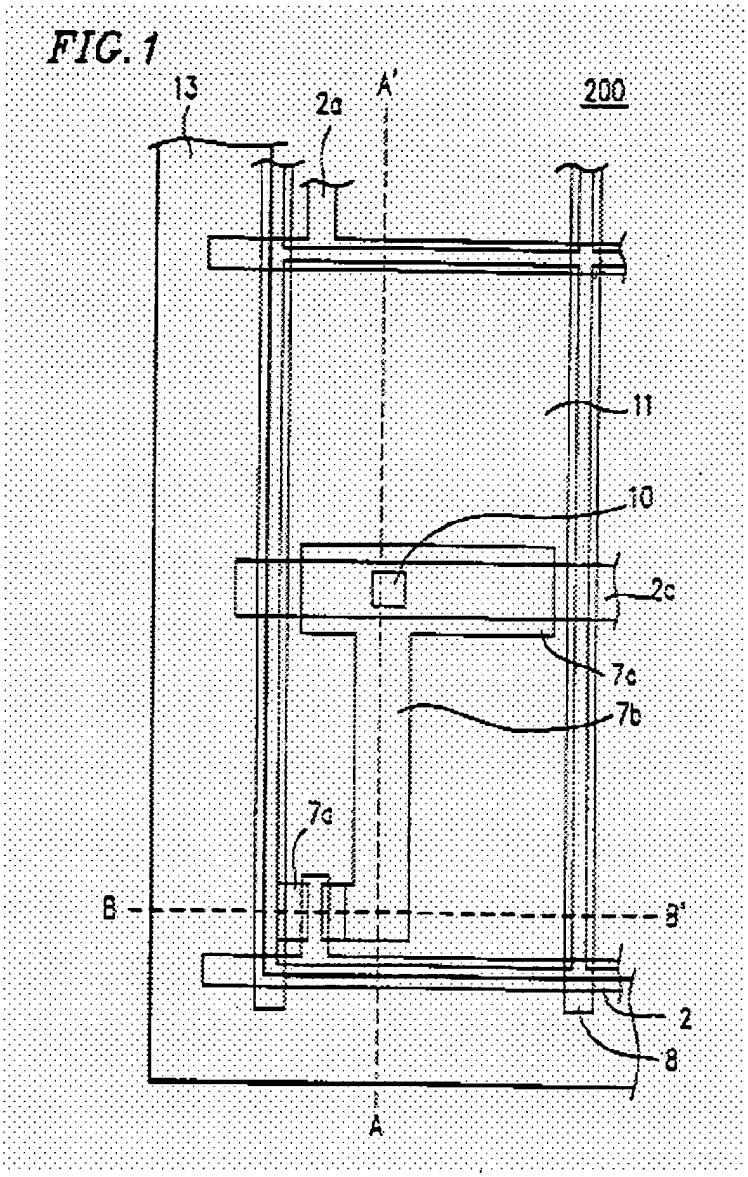
FIG. 10



Tsukada does not explicitly disclose a black matrix defining each pixel; wherein each pixel on a first row has an opening ratio different from that of the each pixel on the rest of the pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer.

Shimada teaches (Title, Abstract, entire patent) a liquid crystal display (LCD) panel comprising:

a first substrate provided with a plurality of gate, 2, and data, 8, lines, the gate lines being arranged to cross the data lines to define a plurality of pixel regions in a matrix arrangement; a second substrate provided with a black matrix layer (col. 5, lines 50-60) to shield portions other than the pixel regions from light; and liquid crystal layer injected between the first and second substrates, wherein the pixel regions in a peripheral portion of the matrix arrangement has an aperture ratio lower than that of the pixel regions in other portions of the matrix arrangement (col. 2, lines 2-12 and col. 6, lines 35-45) in the example where the black matrix overlaps the pixel electrodes, 11 (col. 2, lines 29-42), in areas where no gate or data line exists to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment.



Shimada also teaches in Figure 2 an interlayer insulating film, 9 (Applicant's protective layer) formed over the gate lines and data lines with a plurality of pixel electrodes, 11, formed on said protective layer to allow improved aperture ratio and reduced disclination (col. 7, lines 46-63).

Shimada is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add an opening ratio of each pixel at the first

pixel row is different from the opening ratio of the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment and to allow improved aperture ratio and reduced disclination.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Tsukada with the opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer of Shimada to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment and to allow improved aperture ratio and reduced disclination.

As to claim 4, Shimada, as combined above, teaches formation of the black matrix at the second substrate, both as prior art and as preferred embodiments.

As to claims 9 and 11-12, Tsukada discloses in Figure 10 his fourth embodiment (col. 8, lines 38-62) a liquid crystal display, comprising:

a first insulating substrate;

a plurality of gate lines, 3, formed at the first substrate to transmit scanning signals;

a plurality data lines, 1, crossing over the gate lines to transmit picture signals;

a plurality of pixels defined by the gate lines and data lines, the gate lines dividing the pixel electrode into rows and the data lines dividing the pixel electrodes into columns; a protective layer formed over the gate lines and data lines; a plurality of pixel electrodes, 9, formed on the protective layer, each pixel electrode corresponding to one of the plurality of pixels;

a second insulating substrate facing the first substrate;

a liquid crystal layer injected into the gap between said first insulating substrate and said second insulating substrate; and

a storage capacitor, 7, formed between said pixel electrode and the previous gate line (col. 6, lines 40-48);

a dummy gate line (Applicant's storage capacitor line) formed on said first insulating substrate parallel to the gate line (col. 11, lines 45-68), the storage capacitor line overlapping the pixel electrodes at the first pixel row;

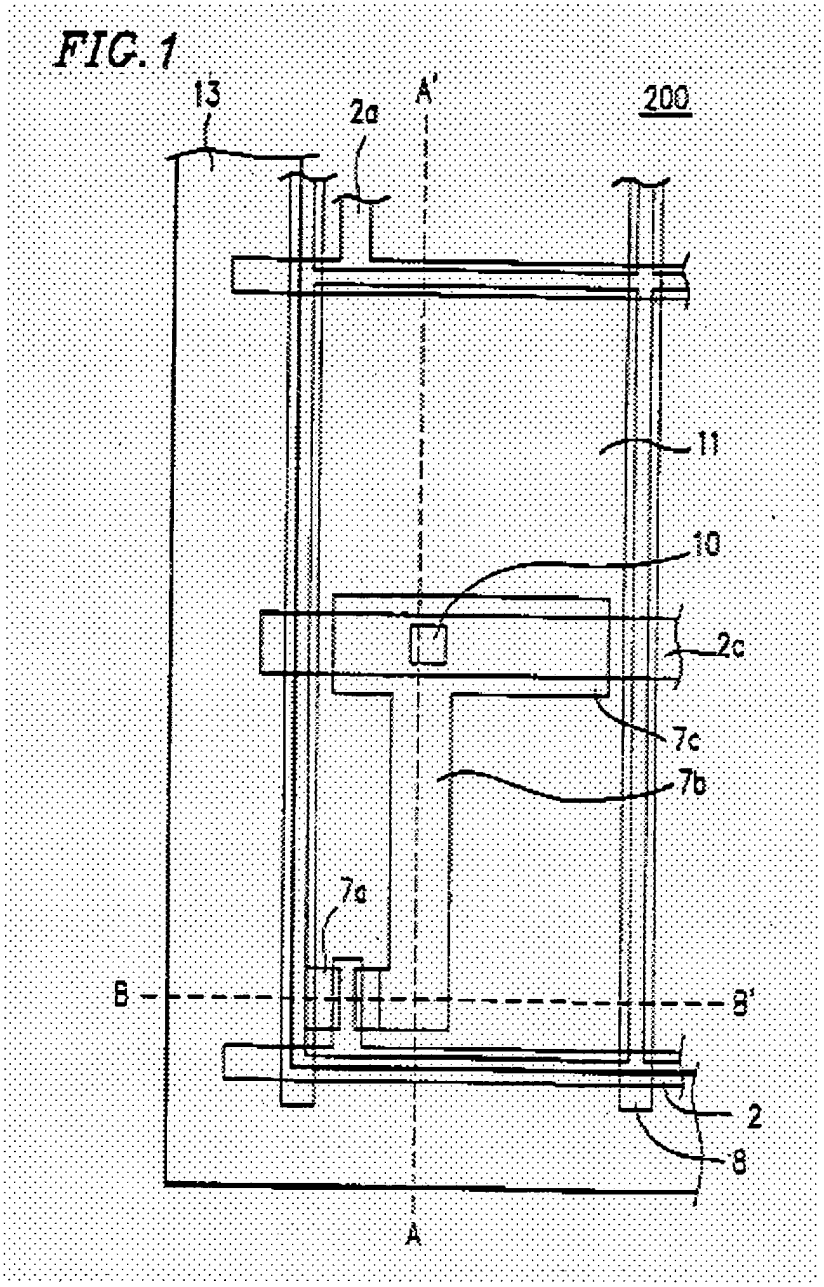
a first storage capacitor formed between said pixel electrode and the previous gate line; and, a second storage capacitor, 7, formed between said pixel electrode and said storage capacitor line;

wherein a gate-off voltage is applied by connecting to the last gate line (col. 11, lines 59-61).

Tsukada does not explicitly disclose a black matrix defining each pixel; wherein each pixel on the first row has an opening ratio different from that of each pixel on the rest of the rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer.

Shimada teaches (Title, Abstract, entire patent) a liquid crystal display (LCD) panel comprising:

a first substrate provided with a plurality of gate, 2, and data, 8, lines, the gate lines being arranged to cross the data lines to define a plurality of pixel regions in a matrix arrangement; a second substrate provided with a black matrix layer (col. 5, lines 50-60) to shield portions other than the pixel regions from light; and liquid crystal layer injected between the first and second substrates, wherein the pixel regions in a peripheral portion of the matrix arrangement has an aperture ratio lower than that of the pixel regions in other portions of the matrix arrangement (col. 2, lines 2-12 and col. 6, lines 35-45) in the example where the black matrix overlaps the pixel electrodes, 11 (col. 2, lines 29-42), in areas where no gate or data line exists to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment.



Shimada also teaches in Figure 2 an interlayer insulating film, 9 (Applicant's protective layer) formed over the gate lines and data lines with a plurality of pixel electrodes, 11, formed on said protective layer to allow improved aperture ratio and reduced disclination (col. 7, lines 46-63).

Shimada is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add an opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment and to allow improved aperture ratio and reduced disclination.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Tsukada with the opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer of Shimada to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment and to allow improved aperture ratio and reduced disclination.

As to claims 13 and 15, Shimada, as combined above, teaches formation of the black matrix at the second substrate, both as prior art and as preferred embodiments.

As to claims 20-22, Tsukada discloses connection of the storage capacitor line to the last gate line (col. 11, lines 59-61) (Applicant's further comprising a gate-off line formed on said first substrate to transmit a gate-off voltage, wherein the gate-off line and said storage capacitor line are formed at the same layer as the gate line, wherein

the gate-off line and said storage capacitor line are electrically connected to each other via a connection member, and the connection member is formed at the same layer as the data line or said pixel electrode).

As to claims 23 and 24, Tsukada discloses a functional liquid crystal display with driving circuitry and voltage driving scheme (col. 11, lines 61-66) (Applicant's further comprising gate signal transmission films arranged at said first substrate and provided with a gate driving integrated circuit that is electrically connected to the gate lines and outputs gate driving signals, and data signal transmission films arranged at said first substrate and provided with a data driving integrated circuit that is electrically connected to the data lines and outputs data driving signals,
wherein a common electrode wire for applying the common electrode voltage (Vcom), a gate-on wire for applying the on-voltage Von to the TFTs controlling the picture signals, a gate-off wire for applying the off-voltage Voff, and wires for transmitting carry-in or gate-clock signals are formed on the edge portion of the first substrate between the gate signal transmission film and the data signal transmission film, wherein the common electrode wire, the gate-on wire, and the gate-off wire at the same layer as the gate lines with the same material).

Allowable Subject Matter

3. Claims 8, 14, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As to claim 8, relevant prior art of record did not disclose, alone or in combination, the liquid crystal display of claim 2, wherein the opening ratio of the first pixel row is designed to be *60-80% of the opening ratio* of the other pixel rows. The closest combination is Tsukada in view of Shimada, but they do not explicitly disclose the claimed range of *60-80%.*

As to claim 14, relevant prior art of record did not disclose, alone or in combination, the liquid crystal display of claim 13, wherein opening width of said black matrix at the first pixel row in the *longitudinal direction of the gate line is identical* to opening width of said black matrix at the other pixel rows. The closest combination is Tsukada in view of Shimada, but they do not explicitly disclose an opening width of said black matrix at the first pixel row in the longitudinal direction of the gate line is identical to opening width of said black matrix at the other pixel rows in a display wherein the

opening ratio set by said black matrix is such that each pixel on a first row has an opening ratio different from that of the each pixel on the rest of the pixel rows.

As to claim 19, relevant prior art of record did not disclose, alone or in combination, the liquid crystal display of claim 11, wherein the opening ratio of the first pixel row is designed to be *60-80% of the opening ratio* of the other pixel rows. The closest combination is Tsukada in view of Shimada, but they do not explicitly disclose the claimed range of *60-80%.*

Response to Arguments

Applicant's arguments filed on 27 October 2004 have been fully considered but they are not persuasive.

Applicant's ONLY arguments are as follows:

(1) Shimada does not teach the use of a black matrix to provide an opening ration different in the first row.

(2) Shimada teaches away from reducing the opening ratio of the pixel on any row.

Examiner's responses to Applicant's ONLY arguments are as follows:

(1) It is respectfully pointed out that Shimada teaches in both the background of the invention (as conventional) and in the summary of invention (col. 2, lines 29-42), per rejections above.

(2) It is respectfully pointed out that Shimada teaches at least one embodiment and discloses the background of the invention wherein the opening ratio of the pixels in the first row is reduced per rejections above. Please consider that a reference should be considered for all that it would have taught to one having ordinary skill in the art. Shimada is considered to be ample teaching of the use of a black matrix as suitable to reduce the opening ratio of the first row of pixels to avoid unwanted light leakage thereby rendering the claimed invention obvious to those having ordinary skill in the art at the time the claimed invention was made.

It is respectfully pointed out that Applicant's arguments are largely those responded to in the Final Rejection. Examiner has taken the applied references as a whole and considered what they would render obvious to one having ordinary skill in the art at the time the claimed invention was made. Please note that such is NOT limited to the specific or preferred embodiments of the applied prior art. Rather, it includes everything that would be redered obvious by the combination of applied prior art given the knowledge and skill of one of ordinary skill in the art at the time the claimed invention was made. For example, a collection of teachings of a plurality of design solutions suitable for reducing the aperture ratio would render them all obvious (render all of the design solutions obvious) for the intended purpose of reducing aperture ratio.

Selection of a specific one of said design solutions would require only routine experimentation in the art.

Please note: Applicant did not amend the claims subsequent to the Final Rejection mailed 27 July 2004, so this rejection could have been made Final. Examiner has made this action Non-Final as a courtesy to Applicant.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy L. Rude whose telephone number is (571) 272-2301. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Timothy L Rude
Examiner
Art Unit 2883

tlr

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